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THESIS

OPTIMIZING SCR DESIGN FOR OPTICAL DETECTION

by

Esperanza Paz C. del Casal

June 2009

Thesis Advisor:	Gamani Karunasiri
Co-Advisor:	Douglas Fouts

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13. ABSTRACT (maximum 200 words)

Though traditionally used as switching devices, thyristors are capable of facilitating the conversion of light intensity to frequency. However, off-the-shelf thyristors are designed to handle relatively large current (> 1 mA) and are therefore not suitable for low-power light detection. In this work, low current (< 1 nA) thyristors were fabricated using the AMI ABN process via MOSIS based on a previous design that was slightly modified. The fabricated thyristors as well as the transistors that were included for verification purposes were characterized with an Agilent 4155B Semiconductor Parameter Analyzer. The fabricated thyristors exhibited the expected switching behavior and operated with current levels in tens of pA. Measured I-V characteristics of the transistors revealed that the exclusion of an active mask even within the pbase layer when using the AMI ABN process results in suboptimal performance. An analysis of the thyristors corroborated this finding and confirmed simulation results in previous work that indicate that the thyristor switching voltage decreases in direct proportion to the width of the first n doped layer. Incident light was also found to cause a decrease in switching voltage. From these findings, the optimal width of the first n doped layer was determined to be equal to or greater than 5.2 μm, and the active mask was recognized as an essential augmentation to all metal contacts in devices fabricated using CMOS technology.

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OPTIMIZING SCR DESIGN FOR OPTICAL DETECTION

Esperanza Paz C. del Casal
Lieutenant, United States Navy
B.S. Biomedical Engineering, University of Rochester, 2003

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June 2009

Author: Esperanza Paz C. del Casal

Approved by: Gamani Karunasiri
Thesis Advisor

Douglas Fouts
Co-Advisor

James H. Luscombe
Chairman, Department of Physics

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ABSTRACT

Though traditionally used as switching devices, thyristors are capable of facilitating the conversion of light intensity to frequency. However, off-the-shelf thyristors are designed to handle relatively large current (> 1 mA) and are therefore not suitable for low-power light detection. In this work, low current (< 1 nA) thyristors were fabricated using the AMI ABN process via MOSIS based on a previous design that was slightly modified. The fabricated thyristors as well as the transistors that were included for verification purposes were characterized with an Agilent 4155B Semiconductor Parameter Analyzer. The fabricated thyristors exhibited the expected switching behavior and operated with current levels in tens of pA. Measured I-V characteristics of the transistors revealed that the exclusion of an active mask even within the pbase layer when using the AMI ABN process results in suboptimal performance. An analysis of the thyristors corroborated this finding and confirmed simulation results in previous work that indicate that the thyristor switching voltage decreases in direct proportion to the width of the first n doped layer. Incident light was also found to cause a decrease in switching voltage. From these findings, the optimal width of the first n doped layer was determined to be equal to or greater than 5.2 μm, and the active mask was recognized as an essential augmentation to all metal contacts in devices fabricated using CMOS technology.

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EXECUTIVE SUMMARY

Previous research conducted on the subject of optical detection using a silicon controlled rectifier—otherwise known as a thyristor—revealed that the tendency of a thyristor to switch at a lower voltage under illumination made it ideal for the type of detection which relies on pulse generation and perhaps even on the frequency of pulse generation. This thesis is a continuation of the body of work aimed at identifying the dimensional parameters which optimize thyristor performance in optical detection.

An earlier thesis postulates that the width of the first n doped layer has the most significant effect on the magnitude of the switching voltage. The author of that work designed and submitted for fabrication a set of thyristors of varying n doped layer widths and device lengths in order to verify these findings. However, time constraints prevented him from analyzing the finished product. In this paper, those thyristors were examined using an Agilent 4155B Semiconductor Analyzer, and errors in chip layout which precluded them from functioning properly were uncovered. The original thyristor design was then modified and resubmitted to MOSIS for fabrication using the AMI ABN process, but in this latest iteration of the device layout, an active mask was placed under all metal contacts in some of the devices, and two transistors were included for verification purposes. These devices were also analyzed using the Agilent 4155B, and the effects of incident light on thyristor performance were examined.

The active mask proved to be a key factor in ensuring device functionality. Specifically, it was found that devices laid out with the active mask unspecified within the pbase layer, as prescribed in MOSIS publications, could not perform properly. Of the thyristors deemed viable, proper performance confirmed the linear relationship between the width of the first n layer and the switching voltage, and experiments with incident light indicate that the switching voltage decreases in proportion to light intensity. The switching voltage is roughly equivalent to the pulse height generated in a sensor circuit, and 5.2 μm was determined to be the minimum allowable width for the first n doped layer.

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I. INTRODUCTION

A. PAST RESEARCH

Research at the Naval Postgraduate School on pulse mode optical sensing featuring a silicon controlled rectifier (SCR)—otherwise known as a thyristor—started with a discovery made by Professor Gamani Karunasiri of the capability of an SCR to generate voltage pulses under illumination (1). The circuit includes an SCR in series with a resistor-capacitor (RC) circuit, powered by a DC voltage supply (see Figure 1 below). Pulsing under illumination occurs with light exposure directly on the second junction of the SCR or with a photodiode attached to the gate (1).

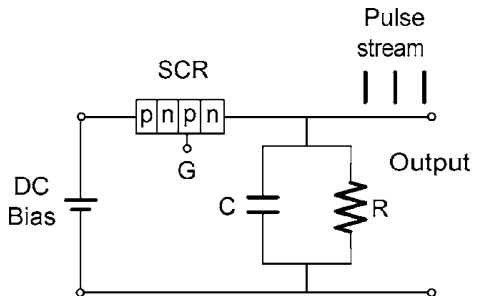


Figure 1. Circuit diagram from (1). G is the gate.

Sustaining pulse mode operation of the circuit primarily involves setting the DC bias to such a level that under illumination the SCR doesn't complete turn-on (1). This state is illustrated in Figure 2 as the interval between the holding current and the switching current. Specifically, it is the condition in which the middle junction of the SCR is never allowed to become forward biased but instead drops the SCR back into the off state from which the device can only ramp up again to its switching point. In other words, the thyristor is kept in a cycle in which it continually begins turning on but never quite finishes the transition.

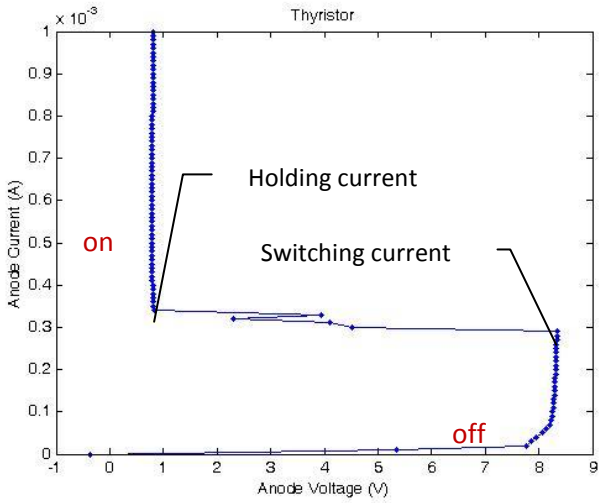


Figure 2. I-V characteristics of Motorola MBS4991-344 thyristor. (After [1]).

The curve in Figure 2 illustrating thyristor behavior can itself be explained by an examination of the p-n junctions included in a thyristor. An external forward bias lowers the built-in voltages at the first and third junctions, thereby lowering the internal electric fields at those junctions. The lowered fields allow holes and electrons to diffuse across the first and third p-n junctions and into the middle p-n junction. The reverse-biased middle junction has a relatively high internal electric field. As illustrated in Figure 3a, this large field pulls holes diffusing into the first n layer from the first p layer and deposits them in the second p layer. Conversely, the large internal field compels electrons diffusing into the second p layer from the last n layer to drift toward the first n layer.

If the external bias is low enough, the large reverse bias at the middle junction will prevent many of the charge carriers drifting across the middle junction from diffusing toward the outer layers just as the large electric field prevents them from diffusing back to where they came. They therefore accumulate in the potential wells depicted in Figure 3b. Those that do diffuse back will only be recycled in a feedback loop that mainly results in further charge accumulation at the potential wells (2).

Eventually, as Figure 3b shows, these accumulated charge carriers will create an electric field across the middle junction that is larger than the initial field and oriented in the opposite direction. This sudden switch in overall field direction will, in turn, cause

the middle junction to become forward biased. All three junctions will then be forward biased, and the thyristor will have reached its holding current and be in an on state (1).

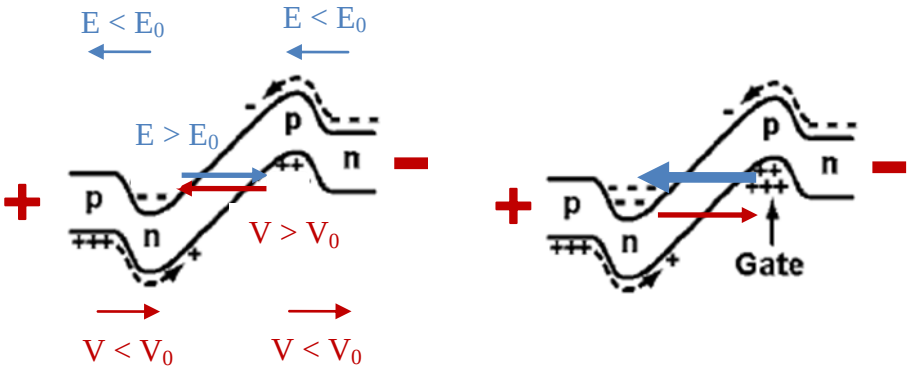


Figure 3. SCR band diagrams showing biases and E fields. (After [1]).

To prevent the thyristor from staying on, a resistor is used to limit the circuit current to a value between the SCR switching and holding current. As the SCR switches, the resulting current flow will charge the capacitor, which subsequently discharges through the resistor as the SCR falls into the off state, thereby providing the necessary conditions for SCR switching. The process thus described repeats and generates a series of pulses shown in Figure 4. The voltage level of the baseline corresponds to the voltage across the resistor due to a steady switching current, and the pulse height is the voltage across the SCR (1).

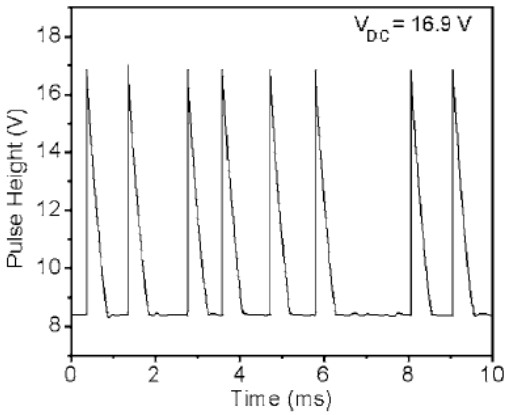


Figure 4. Pulsed output of SCR-centered circuit. (From [1])

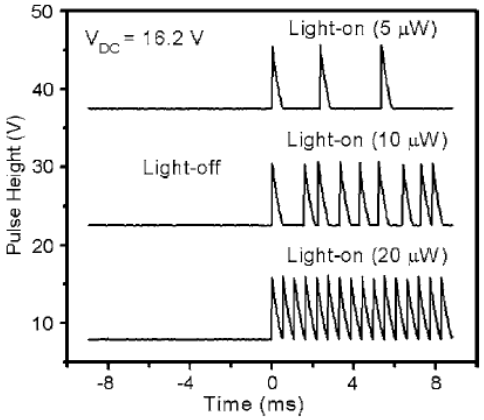


Figure 5. Effects of different magnitudes of light on inter-pulse duration. (From [1])

The existence of a gate current—whether it be through the use of a photodiode in a reverse-biased configuration or through the application of light directly onto the second junction of the SCR—can increase the rate at which the SCR ramps up for switching (1). Figure 5 illustrates the results of Professor Karunasiri's research into the relationship between light intensity and pulse rate. As demonstrated, a greater light intensity translates to a faster pulse rate but has no effect on the pulse magnitude. Furthermore, the inter-pulse duration proves to be variable in all light conditions except that which brings the SCR close to its holding current.

Three important concepts with regards to SCR-centered optical sensors can thus be derived. First, the pulsed response of such a sensor will be of relatively constant magnitude with inter-pulse durations dependent on the applied DC bias—barring the use of the gate contact—rather than on the RC time constant. Second, with a certain fixed DC power supply, the pulse rate will increase in proportion to the light intensity directed at the gate region. Third, the sensor's threshold for the amount of light that will produce a pulsed response is dependent on the gate current needed to induce SCR switching (1).

B. APPLICATION OF PULSE-MODE CIRCUITS AND SCR DESIGN

Subsequent to the original research explored in the previous section, two previous students developed different methods for using SCR-based optical sensors on robotic

platforms, and one student explored the parameters of an SCR which makes it ideal for optical detection. LT Antonio Matos's mobile robots were rigged with SCR-based sensors in such a way that they swarmed toward a light source (3), while LT Ioannis Siganos's mobile robots responded not just to illumination in general but to illuminated numerals in particular (4). LT David Moore submitted for fabrication a chip comprised of multiple SCRs of varying layer dimensions in an effort to identify the means of optimizing SCR performance in optical detection (5). Most of his thesis, however, was dedicated to device simulations since fabrication could not be completed in time.

A characterization of Moore's fabricated SCRs follows in the second chapter, but it would be worthwhile to first review the main points in Moore's thesis and the differences between the actual devices that were manufactured and the simulated device from which Moore developed his conclusions on thyristor behavior.

1. Simulation

Moore's device, depicted in Figure 6, consists of a vertical stack of four semiconductor layers. Simulations based on this structure led to a confirmation of the physics behind SCR operation briefly described in Section A and to the determination that impact ionization is not a significant factor in thyristor switching. More importantly, however, it enabled Moore to categorize the dimensional parameters that favorably affect SCR behavior in an optical detection mode.

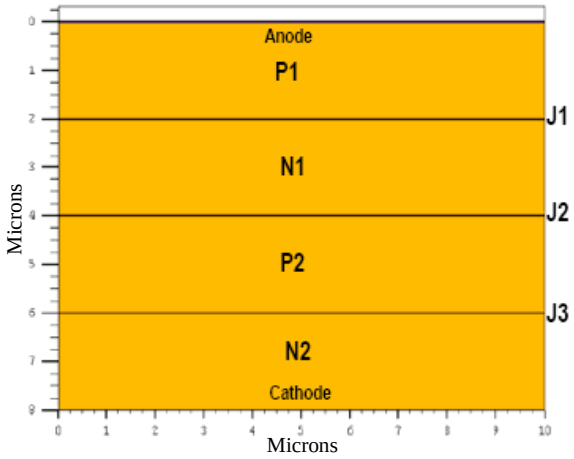


Figure 6. Moore's simulation device. (From [5]). P1 refers to the first p type layer, P2 to the second p layer, N1 to the first n layer, and N2 to the second n layer.

Table 1 describes how device parameters affect the holding current and the switching voltage. For the holding current, lowering the P1 and N2 doping or increasing the P2 doping has a bigger impact. For the switching voltage, increasing the N1 doping or the N1 thickness has a bigger impact. But given the fact that a chip designer has no control over the exact doping of the semiconductor layers, the only parameter that can realistically be controlled is thickness. It is most likely for this reason that Moore's fabrication design focused primarily on variations in N1 thickness, toward which his SCR simulations incidentally had the most sensitive response.

In general, he found that the most effective means of manipulating the switching voltage depended mostly on N1 doping and thickness and P2 doping (5 p. 51). The switching current, on the other hand, will likely be most affected by P1 and N2 doping since these layers contribute the most to the potential wells formed at N1 and P2 (2).

Table 1. SCR Optimal Parameters. (After [5])

HIGHER HOLDING CURRENT			**HIGHER SWITCHING VOLTAGE**		
	Doping	Thickness		Doping	Thickness
P1	↓		P1	↓*	
N1	↑*	↑*	N1	↑	↑
P2	↑	↑*	P2	↑*	↑*
N2	↓		N2	↓*	

* Denotes lesser effect

From a basic understanding of thyristor operation, Moore designed a set of SCRs which he then submitted for fabrication using the MOSIS foundry service (5). After determining layer doping concentrations based on resistivity values from previous MOSIS fabrications runs and estimated layer thickness based on comparisons with similar CMOS processes (5 pp. 55-56), he generated the I-V curves in Figure 7 using a

SILVACO finite element simulator. The legend describes N1 widths in microns. Note that the longer width produces a larger switching voltage. Also note that the simulation curves are in Amperes per μm.

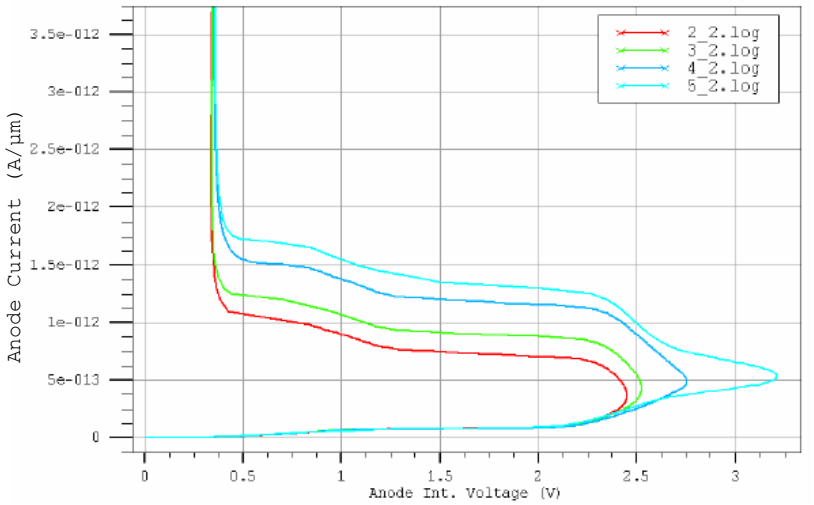


Figure 7. Moore's Atlas simulation for fabricated SCRs. (From [5]).

2. SCR Fabrication

Moore chose MOSIS as the vehicle for chip fabrication because they were—and still remain—the most affordable alternative. He chose the AMI ABN process because it allows for bipolar devices; although, the process is mostly geared towards CMOS-based integrated circuit fabrication. Chip layout was accomplished via Tanner Inc.'s L-Edit program (5).

The chip consists of one substrate contact, one group of 110 μm length SCRs, and one group of 510 μm length SCRs. In each of these two groups there were two SCRs with 2.2 μm, 3.2 μm, 4.2 μm, and 5.2 μm N1 widths. The devices with 2.2 μm N1 widths are outside of the prescribed design rules, so one can only assume that they were included as a test to see how design rule restrictions could affect device behavior. 3.2 μm is the actual minimum limit for the distance between the layers designated as N1 and P2

(5 pp. 59, 61). Some bond pads were left unused, and all the devices share one bond pad for the anode contact (P1), one bond pad for the cathode contact (N2), and one bond pad for the gate contact (P2). See Figure 8.

The bond pad setup ultimately proved to be an unfortunate design error. An examination conducted by Professor Karunasiri on the chip layout after it was already submitted for fabrication revealed a faulty connection between the anode contact and the gate contact in one of the devices. Since all the devices essentially share access to external voltage, all the devices can then be considered to have the same wiring flaw.

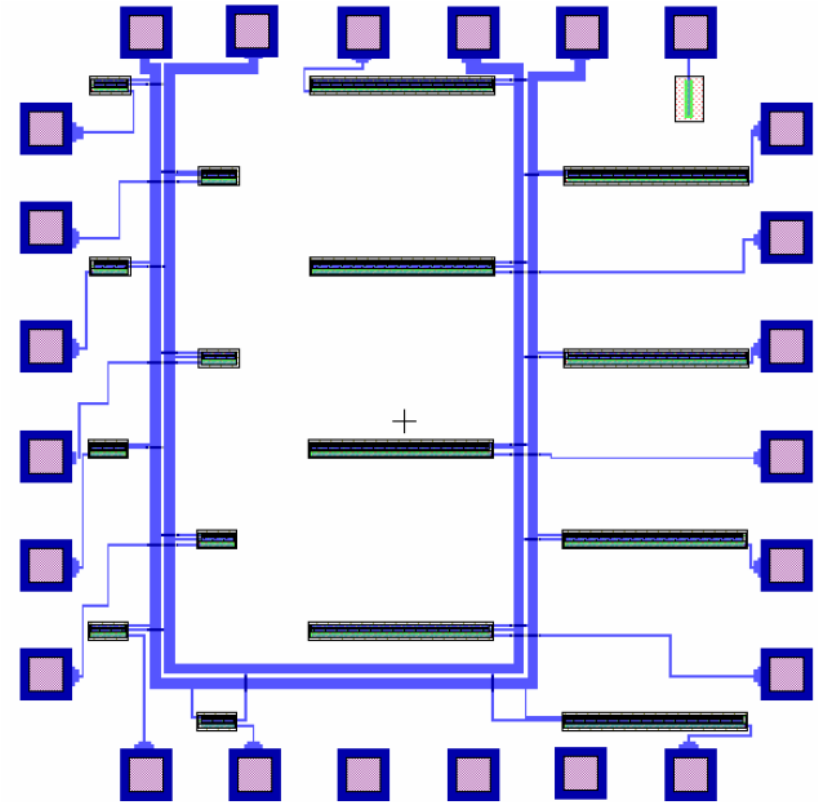


Figure 8. Moore's fabricated chip. (From [5])

II. FABRICATED SCR DESIGN AND CHARACTERIZATION

A. PREVIOUSLY FABRICATED CHIP TEST RESULTS

1. Device Behavior

To eliminate the faulty wire connection between the anode and the gate, a reverse bias (negative voltage on the anode contact) was applied across the two terminals until the wire was fused. This occurred at approximately 0.4 Amperes.

The following measurements were made with an Agilent 4155B Semiconductor Parameter Analyzer and accompanying Agilent 16442A Test Fixture with appropriate socket module. For the analyzer to handle a multi-valued current function, the source/monitor unit (SMU) for the anode contact had to be set to current mode with variable function while the SMU for the cathode contact was set to common mode with constant function. All other unused SMU's were disabled by deleting the rows on which they are displayed. These settings are in the 'Channels' page and should be set after choosing the default measure setup on the right-hand menu. In the 'Measure' page, the analyzer was left on single sweep mode with linear log. To maximize the number of data points generated, compliance was set to 100 V, and power compliance was set to 2 W. Table 2 summarizes the equipment setup.

Table 2. Agilent 4155B setup for SCR measurement. Gate contact open.

Channels	Configuration (right-hand menu)		Pin	Mode	Function
	Default Measure Setup	SMU1	8*	I	VAR1
		SMU3	7*	COMMON	CONSTANT

Measure	Sweep	Log	Start	Stop	Step	Compliance	Power compliance
	Single	Linear	0 A	6 nA	60 pA	100 V	2 W

*Dependant on device. SMU1 reserved for anode contact, SMU3 for cathode contact.

Measuring the devices after the wire burning produced I-V curves which do not portray thyristor behavior. Figure 9 is offered as an illustration, but all the devices on the chip tested behaved the same way under this particular measurement and in the subsequent measurements to be discussed shortly.

The equipment's max compliance is 100 V, which manifests itself in a seeming breakdown of the device at that voltage. As expected, current increases as more voltage is applied, but at no point is there a period of negative resistance followed by device turn-on. Application of 20 V on the substrate contact (via SMU2, mode V, function constant) merely shifts the entire curve left if negative voltage is applied or right if positive voltage is applied (effect not shown). 20 V DC is the maximum voltage allowed by the equipment for a constant function setting.

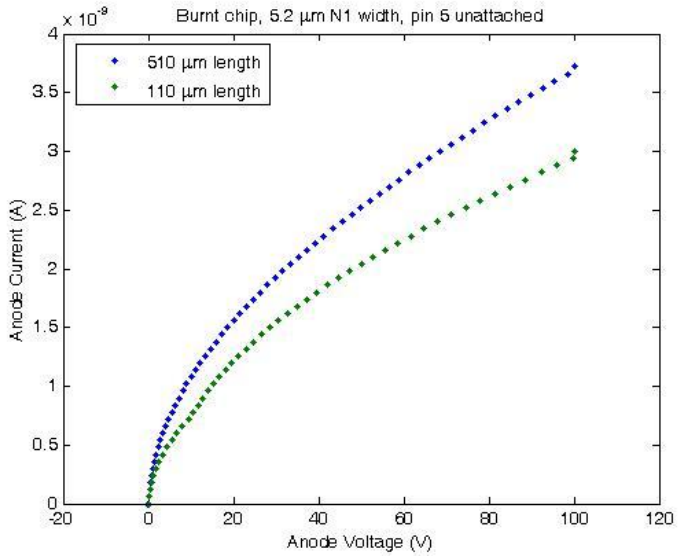


Figure 9. SCRs under forward bias. Two devices of differing lengths are compared here.

The same behavior persists even under reverse bias. The two devices compared in Figure 10 show a closer change in current, but the general trend is the same under reverse bias as it is under forward bias for all the devices on the chip.

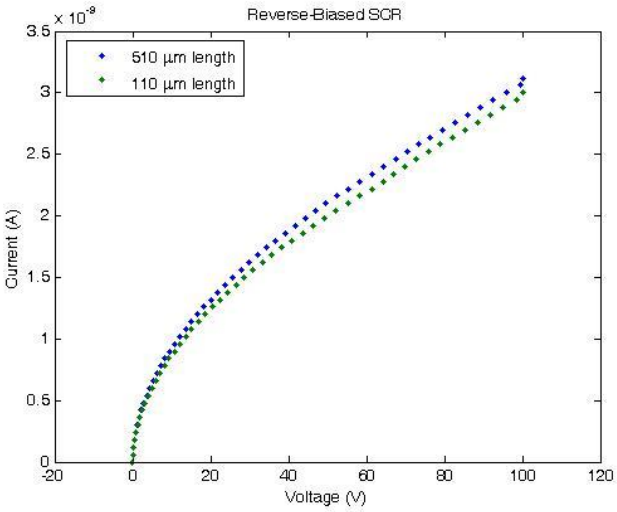


Figure 10. SCRs under reverse bias. Two devices of differing lengths are compared here, both with 5.2µm N1 widths.

Similarly unexpected behavior is also evident between the anode and the gate (see Figure 11). Under both forward and reverse bias, there is an increase in current until the equipment's max compliance is reached, but this growth should be exponential in the manner of p-n junctions and should be evident near 1 V—well before the equipment max compliance of 100 V. The behavior of one device is shown here because all the others behaved in the same way.

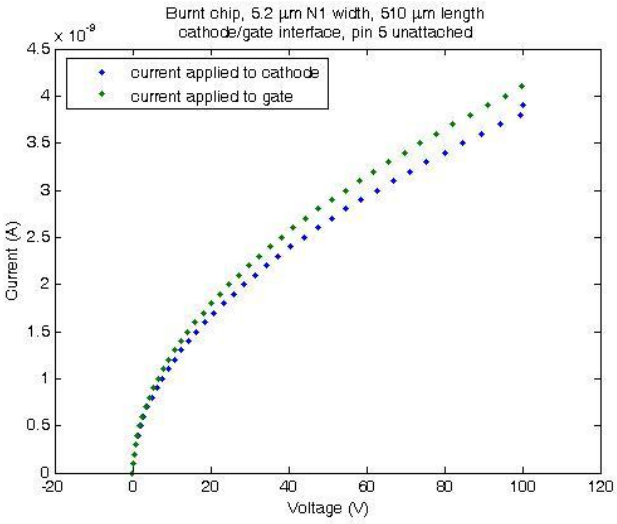


Figure 11. SCR under forward and reverse bias alternately.

2. Analysis

The consistently unexpected and identical behaviors noted above suggests a general device failure due to either chip damage from the wire burning or a particular element of the original design which cannot be identified without examining the design rules check (DRC) error logs. Due to the lack of a non-disclosure agreement between NPS and MOSIS, Moore could not use the DRC feature on L-Edit and perform a design rules check, so there are no actual error logs to examine. Any further productive analysis of Moore's SCR devices must now therefore be restrained to the elimination of the possibility of equipment error being the cause of the discrepancies noted between expected and actual device behavior.

With this goal in mind, the I-V characteristics of a bi-directional thyristor and a silicon photodiode were obtained (see Figure 12 and Figure 13) using the same semiconductor parameter analyzer with which the fabricated devices were tested.

Figure 12 clearly shows the snap-back region associated with thyristor turn-on. The lines connecting the data points are included to provide a better visual and are not meant to be interpreted as best-fit curves.

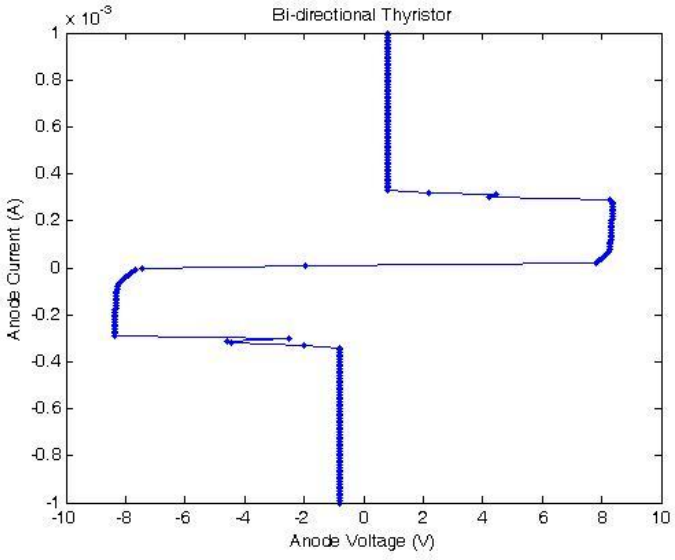


Figure 12. I-V characteristics of Motorola MBS4991-344 thyristor.

The silicon photodiode also behaved as anticipated (see Figure 13). The exponential growth expected of diodes is evident starting at around 0.5V. In this measurement, negative bias was also applied to illustrate the breakdown voltage, but the equipment detected only one value before automatically quitting.

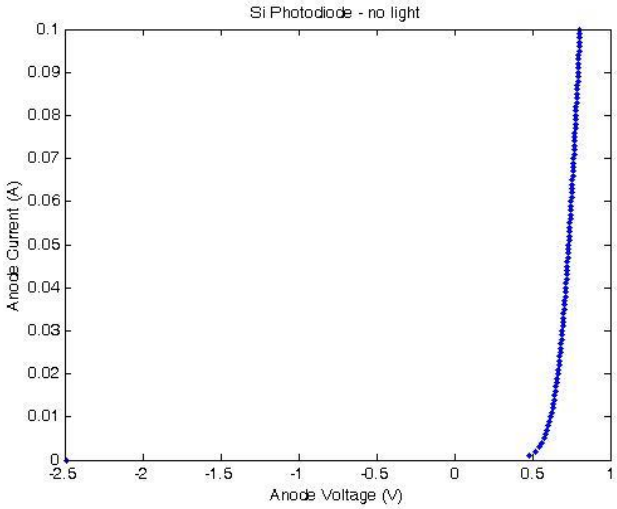


Figure 13. I-V characteristics of FDS1010 Si photodiode with no light exposure.

The expected photodiode behavior under light exposure, shown in Figure 14, was also captured. A microscope illuminator with three intensity settings was used as the light source since more precise control of light energy was not necessary. Predictably, initial photodiode current values ranged according to light intensity with the highest setting generating the highest magnitude of current and the lowest setting generating the lowest magnitude of current.

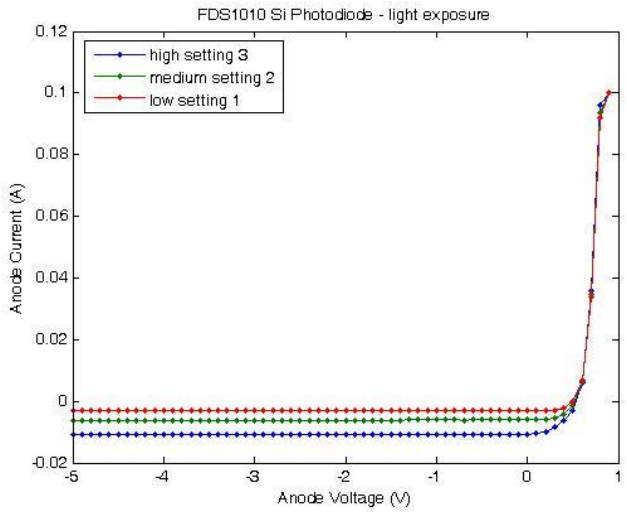


Figure 14. I-V characteristics of FDS1010 Si photodiode with light exposure.

The fact that professionally designed and fabricated devices behaved as predicted when tested by the same equipment used to test the custom-designed devices suggests that the gross discrepancies noted between theoretical behavior and actual behavior in the custom-designed devices must be attributed not to the testing equipment but to the design itself.

B. NEW CHIP DESIGN

1. Manufacturing and Layout

Because of their competitive rates, MOSIS remained the manufacturing gateway of choice for this project. The 1.50 μm ABN CMOS process by AMI Semiconductor, Inc.—now ON Semiconductor—which Moore chose was also chosen for this project in order to expedite the design process (his original design for each device was never fully abandoned—only improved upon). It should be noted that the last multi-project wafer run for this process was on 23 February 2009. L-Edit by Tanner, Inc., was used for

laying out the chip, and the MOSIS SCMOS design rules were applied because they are more conservative than the AMI design rules (6 p. 130) and accessible to the public online.[1]

The new chip layout, limited by the 28-pin package used for mounting the chip, is comprised of eleven devices and seven substrate contacts. The three smaller devices on the top left of Figure 15 are all 110 μm in length with the first having an N1 width of 3.2 μm, the second an N1 width of 4.2 μm, and the third an N1 width of 5.2 μm. This variation is consistent with Moore's original intent of testing the effects of varying N1 widths on the switching voltage. Further variations are provided by the larger devices on the bottom left of the layout. These are all 510 μm in length with the same differences in N1 as the 110 μm devices.

The two SCRs at the bottom of the layout and the one at the bottom right are the same in dimensions as the three at the top left. They were isolated as a precaution against accidental wire bonding between the metal layers extending from the bond pads giving access to all six devices' anodes, gates and well contacts. As shown in Figure 15, the isolated devices have individual bond pads for cathodes, anodes, gates, and well contacts. Except for the middle device, they are unlike the three devices at the top left by a slightly different layering composition. The two devices at the top right are NPN transistors. The one to the right was created using the design supplied by MOSIS on their website (7). The one to the left utilizes the same altered layering composition mentioned above. These devices were added to the chip for verification purposes—i.e., if both the professionally designed transistors and the student-developed SCRs don't behave as expected, then the problem is in the fabrication rather than the design. More substrate contacts than in the original chip were added to ensure that the effects of applying voltage to the substrate could reach the device being tested (8).

[1] Our own non-disclosure agreement with MOSIS was on the individual basis since NPS, as a government facility, is not allowed to sign NDAs. However, for full access to the process's design rules, a full NDA is required. Therefore, this project had to be limited to using the more accessible SCMOS design rules, which are freely published online.

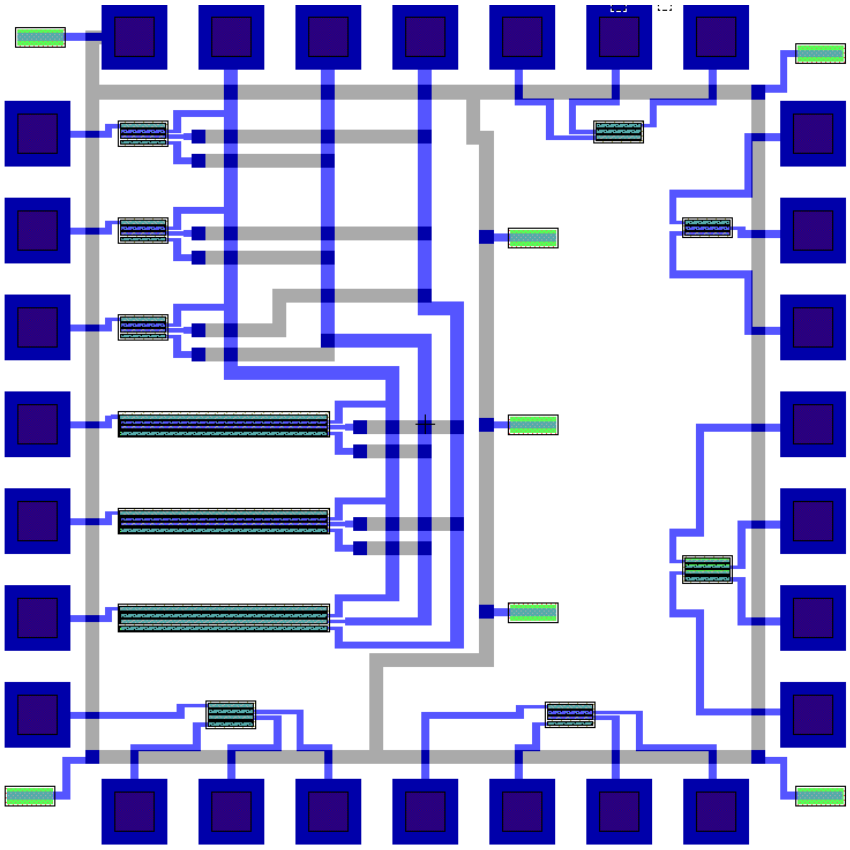
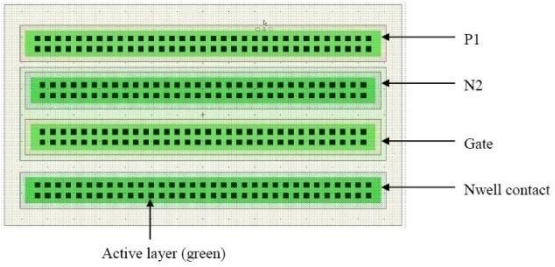


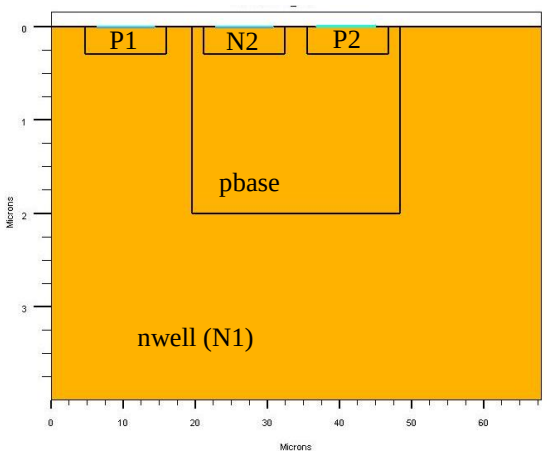
Figure 15. Chip layout submitted for fabrication.

The device layouts were only slightly changed from the original design (see Figure 16a). The N1 widths were adjusted when it was realized that the original measurements for these widths were made from the pbase layer of P2 to the p+ select layer of P1 rather than to the active mask within p+ select.[2] A well contact was added to gain access to the nwell (otherwise known as N1) in case unexpected device behavior prompts a more extensive analysis. More metal contacts (the small black squares) were also added to ensure good conductivity.

[2] For a description of these layers and ones that will be mentioned in the following pages, refer to the MOSIS website (7) or Moore's thesis (4).



(a)



(b)

Figure 16. SCR layout. (a) top view. (b) side view of the SCR used for ATLAS simulation (after (5)) not showing nwell contact.

2. Important Lessons in CMOS Design

Although an in-depth discussion of the design rules and the fabrication layers used are prohibited, there are a few fundamental facts in CMOS design which the trials of completing this project have proved particularly noteworthy.

a. Grid Size and Orientation

When laying out a chip for a particular fabrication process, it's best to keep the grid of the layout program at the standardized size for that process. Since MOSIS design rules are scalable so that designs can easily be transferred to different processes (6 p. 130), layout programs like L-Edit also have a grid scaling feature which allows one to design at the appropriate process scale. However, designing in other than the default scale will likely cause device elements to be off the manufacturing grid. This could have a significant impact on device performance.

b. Wide Metal Spacing

No maximum restrictions *usually* exist with regard to metal widths, so for many processes metal connections can be drawn as wide as the designer wants. However, with very wide metal layers (e.g., widths in excess of 10 μm) certain fabrication processes may require that no less than a particular amount of spacing

between metal conductors is observed. This spacing will likely be greater than the spacing allowed for smaller-sized metal conductors. Some processes may even have a limit on how wide or with what spacing metal conductors can be made (6 pp. 128-129).

c. The Active Mask

In most processes, the active mask is used to indicate where diffusion is to take place (6 p. 126). Essentially, it specifies an area where the field oxide should be etched away so that ion implantation can occur. Including this mask wherever metal contacts are placed is especially important to ensure an electrical connection between the metal and the silicon substrate (8).

If the SCMOS design published online for an NPN transistor (7) is anything to go by, including this mask within pbase is neither required nor recommended since the fabricator is assumed to automatically include the active mask wherever pbase is specified (8). Advice from Professor Karunasiri's integrated circuits designer colleague inspired the effort to test the effects of including an active mask within pbase for the ABN process, keeping in mind that the restrictions imposed by SCMOS design rules might be more conservative and therefore might not apply in this case. Without access to the ABN design rules, one cannot know for sure until faced with physical evidence.

Consequently, one of the NPN transistors was laid out according to SCMOS design rules, and the other was deliberately modified so that an active mask coincided with all metal contacts in the device, even within pbase. With the exception of the 4.2 μm N1 width device, the isolated SCRs at the bottom of the chip as well as the lowest placed 510 μm length SCR were also laid out with the latter changes, while the first five at the top left of the chip were left with the same layering composition as the originals.

C. NEWLY FABRICATED CHIP TEST RESULTS

1. Device Behavior

a. Transistor Measurements

Measurements for the NPN transistors alone proved conclusively the importance of stipulating the occurrence of an active mask in conjunction with all metal contacts in a device fabricated with the ABN process. Figure 17 shows the I-V characteristics of the NPN transistor laid out according to the SCMOS design rules. Lowering or raising the base current range or changing the intervals between base currents did not improve thyristor behavior, and the collector current level remained extremely small.

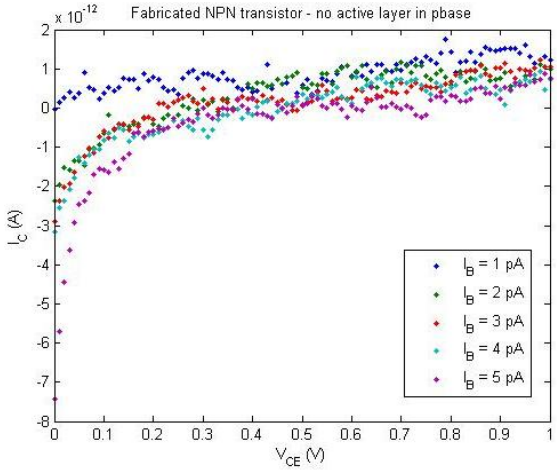


Figure 17. NPN transistor with no active mask in pbase.

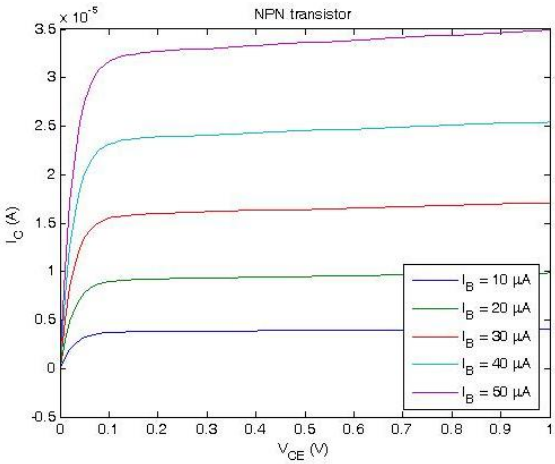


Figure 18. The I-V characteristics of a 2N2222 NPN transistor.

Figure 18 describes the I-V characteristics of an off-the-shelf NPN (2N2222) transistor, while Figure 19 represents the I-V characteristics of the transistor fabricated with an active mask within pbase. A comparison of the performance of all three transistors suggests better transistor operation with the deliberate specification of active masks at all metal contacts as opposed to without.

When measured like an SCR where current is applied instead of voltage (to accommodate equipment limitations in handling current snap-back) and the base contact is largely ignored, the transistor with no active in pbase behaved more like the

damaged SCRs in Section B. Those particular devices also had the same layering composition. The transistor with active in pbase, on the other hand, displayed behavior characteristic of transistors approaching an infinite emitter current gain (9 p. 175). Figure 20 illustrates the differences between the two. Extending the voltage range of Figure 19 to 1 V would show the same curve as the transistor with active in pbase in Figure 20.

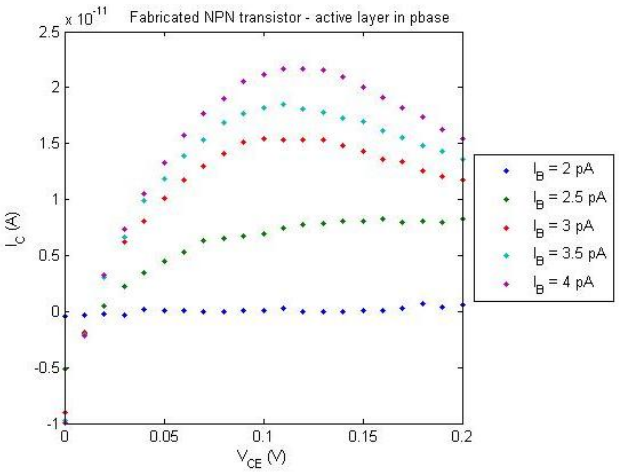


Figure 19. NPN transistor with active mask in pbase.

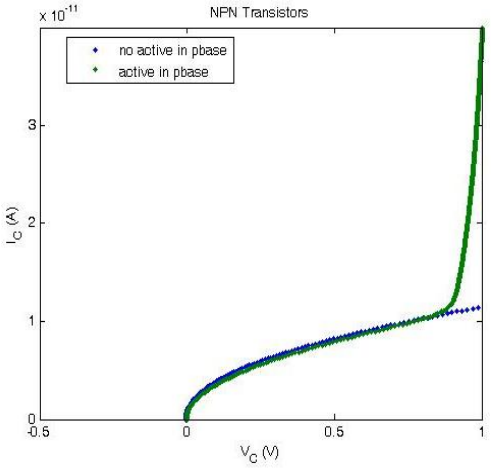


Figure 20. NPN transistors with I_B=0.

The most definitive proof of the active mask's importance is evident in the p-n junction performance of the transistors lacking this implementation within pbase. In the device without active in pbase, the junctions between the base and the collector and between the base and the emitter performed in a manner unlike a diode. Figure 21 illustrates their identical behavior. On the other hand, those same junctions in the transistor with active in pbase performed as in Figure 22, which is representative of classic diode behavior and therefore an expected outcome.

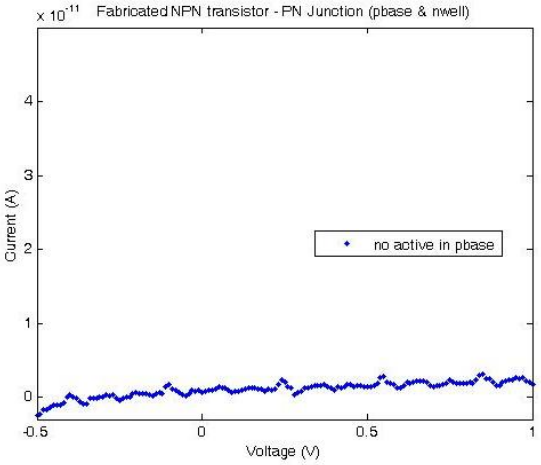


Figure 21. Base/collector junction in transistor without active in pbase.

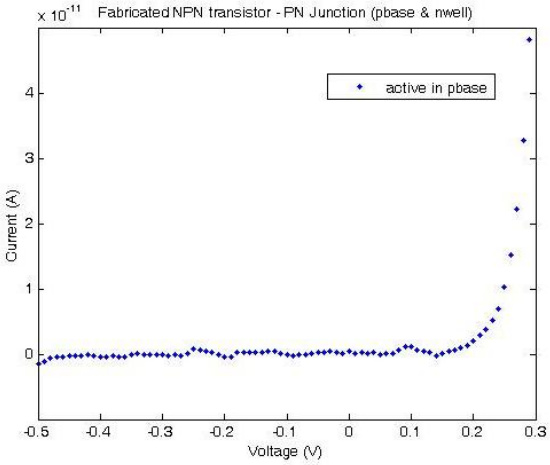


Figure 22. Base/collector junction in transistor with active in pbase.

Equipment configuration for regular transistor measurements involved the use of the MEM1 preset channels setup (in right-hand menu in the 'Channel' page) on the same Agilent analyzer used for the old chip. The contact for the first nwell is the collector, the contact for the n+ select layer within pbase is the emitter, and the contact for the p+ select layer in pbase is the base. When measured as an SCR, the setup in Table 3 was used with the collector contact in place of the anode contact, the emitter contact in place of the cathode contact, and the base contact not used at all. Junction measurements were done using the MEM4 preset configuration.

b. SCR Measurements

For the SCR characterizations, the same Agilent equipment was set up according to Table 3. The line for SMU3 was deleted if no gate current was applied, and the mode and function were changed to V and CONSTANT respectively when voltage was applied to the substrate. This Channels setup is different from the setup used for the original SCRs only in the use of SMU2 and SMU3 for gate current, but these two source/monitor units are interchangeable and using one over the other should not affect the results (10). Junction measurements for the SCRs also involved the use of the MEM4 preset button.

Table 3. Agilent 4155B setup for newly fabricated SCRs.

Channels	Configuration (right-hand menu)						
				Pin	Mode	Function	
	Default Measure Setup			SMU1	18*	I	VAR1
				SMU2	21*	COMMON	CONSTANT
				SMU3	20*	I	CONSTANT
Measure	Sweep	Log	Start	Stop	Step	Compliance	Power compliance
	Single	Linear	0 A	40 pA	100 fA	2 V	OFF

*Dependant on device. SMU1 reserved for anode contact, SMU2 for the cathode contact, and SMU3 for the gate contact.

In general, the results of the SCR measurements proved rather promising. Though none of the SCRs consistently generated the same I-V curve—showing instead a gradual degradation of switching voltage during consecutive measurements—all the devices except the isolated 4.2 μm N1 width device displayed characteristic thyristor behavior in which a maximum voltage is followed by reverse resistance and, finally, device turn-on.

Figure 23 is of the 110 μm length SCRs, and Figure 24 is of the 510 μm length SCRs. The most consistent behavior—in terms of predicted switching voltage and switching current—in either length is displayed by the 4.2 and 5.2 μm N1 widths. Moore's simulation (see Figure 7) indicates that both parameters should be higher for the 5.2 μm width than for the 4.2 μm width, and this notion is consistent with the measurements. The 3.2 μm N1 width device, on the other hand, should have the lowest values for these parameters, and it clearly does not in the 510 μm length device. Moreover, the current range for the 510 μm length SCRs are not significantly higher than that of the 110 μm length SCRs.

One other inconsistency worth noticing is the marked difference in the holding voltage of the 5.2 μm N1 width SCR and the other devices with the same 510 μm length. This difference does not appear in the 110 μm length devices. However, none of the 110 μm SCRs characterized in Figure 23 has an active mask included within pbase, and the device in question with a length of 510 μm does.

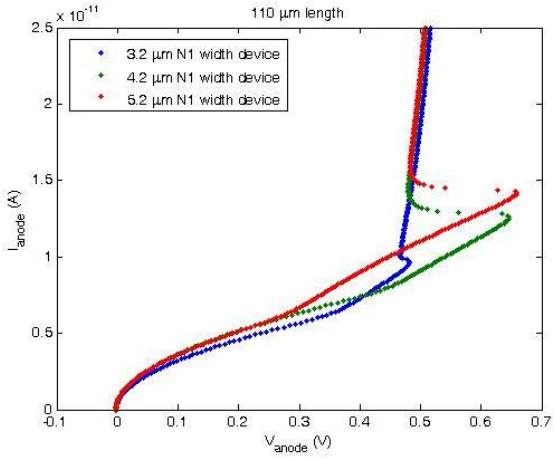


Figure 23. 110 µm length SCRs with different N1 widths.

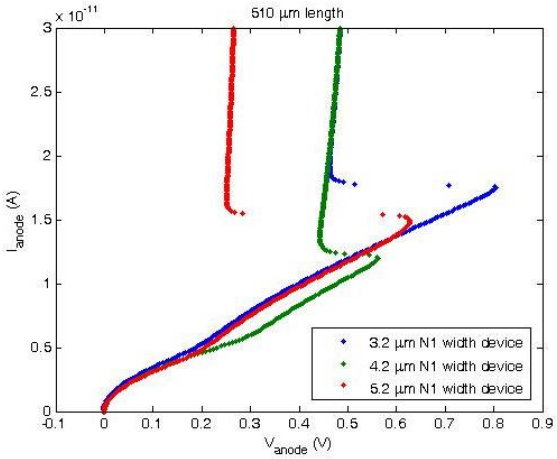


Figure 24. 510 µm length SCRs with different N1 widths.

Of the three SCRs with modified layering configurations only two were 110 µm in length and isolated and only one was 510 µm in length, so the number of comparisons that could be made was limited. Nevertheless, the difference between the I-V curves of the 3.2 and the 5.2 µm N1 widths (see Figure 25) is consistent with Moore's simulation results since the switching currents and the switching voltages are lower for the shorter width.

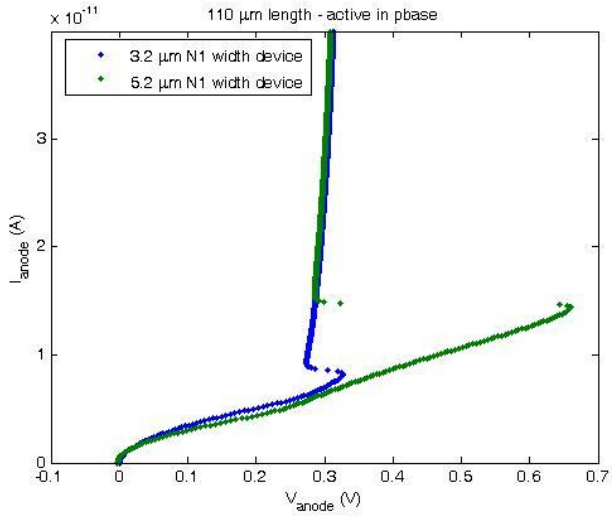


Figure 25. 110 µm length SCRs with active in pbase. These are isolated devices of differing N1 widths.

The properly configured 110 μm length devices with 3.2 and 5.2 μm N1 widths achieved lower holding voltages than devices of similar lengths with no active mask in pbase (see Figure 26 and Figure 27), as foretold by the behavior noted in Figure 24. Note also the larger difference between the switching and the holding voltages in the devices with active. The effect is most pronounced in the wider N1 width.

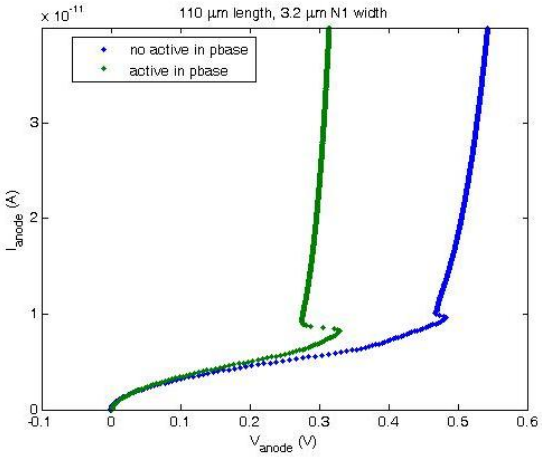


Figure 26. I-V characteristics of 3.2 μm N1 width SCRs, 110 μm length.

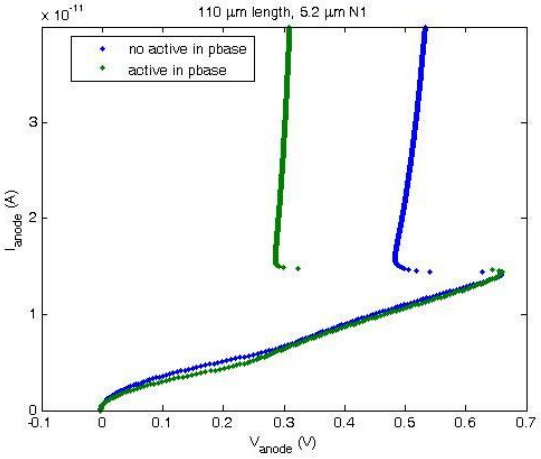


Figure 27. I-V characteristics of 5.2 μm N1 width SCRs, 110 μm length.

The 5.2 μm N1 width, 510 μm length SCR cannot be easily compared to other devices of the same length since the others were laid out according to the original SCMOS design rules. Even so, as mentioned above, the lower holding voltage apparent in Figure 24 can probably be attributed to the incorporation of active within pbase since the 110 μm length devices in Figure 23 all lack this implementation and consequently produced nearly the same holding voltages.

The SCR with a 5.2 μm N1 width and a 510 μm length may also be compared to its 110 μm length counterpart to provide insight into the effects of length in devices which are otherwise identical. The difference between the holding and the switching voltages—approximately 0.4 V according to Figure 28—is basically the same in both cases, but the longer length operates at a lower voltage range. The holding and switching currents are also similar in both cases even though the devices differ in area by a factor of five. A later section will reveal that the manner in which the 510 μm length

SCR is connected to the other devices in that part of the chip prevents any measurements from being taken that do not inadvertently bias the substrate.

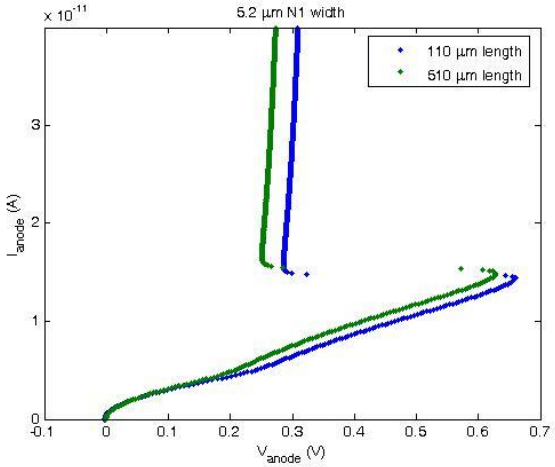


Figure 28. 5.2 µm N1 width, different lengths.

Under reverse bias, the isolated 5.2 µm N1 width SCR underwent avalanche breakdown at approximately 20.9 V and 75 pA (see Figure 29). The equipment's max compliance was set to 25 V, which means that the vertical line at 20.9 V is not an effect of the measuring apparatus but indicative of actual device breakdown.

If P2 and N2 are heavily doped and the junction between them goes into avalanche breakdown early enough that the breakdown of the whole thyristor is dependent on the junction between P1 and N1 (two-transistor model), then the breakdown voltage of the thyristor can be described by (9 p. 191)

$$BV \cong 5.34\times10^{13} N_{N1}^{-3/4}$$

where N_{N1} is the doping concentration of the N1 region in units of cm^{-3}. This equation also assumes a heavily doped P1 layer with an abrupt junction. If diffusion only occurs within the active mask and the select layers merely specify the type of diffusion that should take place (6 p. 126), then the P1/N1 junction can be reasonably considered abrupt.

Using the measured value of BV, N_{N1} is calculated to be approximately 3.5×10^{16} cm^{-3}, which is about a factor of two higher than Moore's estimation of 7×10^{15} cm^{-3} (5 p. 57). A comparison with actual doping values would be interesting if such access can be arranged.

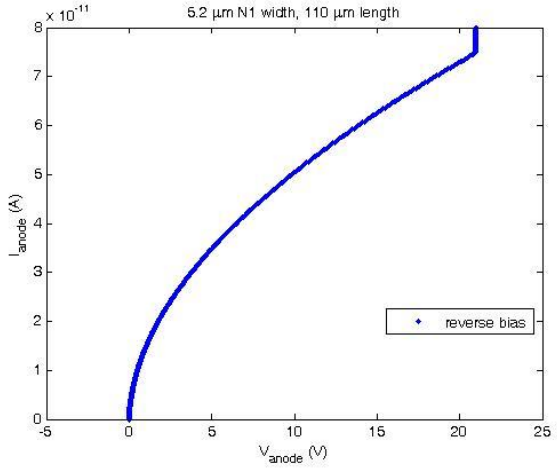


Figure 29. I-V characteristics of SCR with 5.2 µm N1 width and 110 µm length under reverse bias.

Of the three isolated SCRs, only the SCR with a 4.2 µm N1 width failed to generate thyristor I-V characteristics. In Figure 30, there is a noticeable lack of a reverse resistance associated with distinct switching and holding voltage levels. The device deficiency is most likely due to the fact that its design layout precluded the specification of an active mask within pbase. This conclusion is made in light of the fact that even the SCR with a shorter N1 width is capable of functioning as a thyristor, and accidental violations of the design rules are therefore unlikely causes of degraded viability.

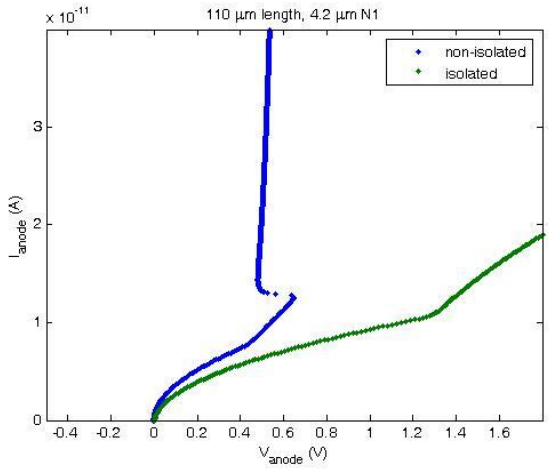


Figure 30. SCRs of the same dimensions, but one with a defect. Equipment max compliance was 2 V.

c. Effects of Biasing the Substrate

The introduction of voltage to the substrate contact was initially undertaken to see if doing so would improve thyristor performance by minimizing junction formation between the substrate and the nwells to which it is adjacent. The actual composition of the substrate is unknown, however, and its interactions with the devices above it are only theorized possibilities. Unfortunately, rather than improving device performance, substrate bias reduced a viable SCR into a device resembling the defective SCRs above. It was later found that these manipulations were actually unnecessary—even detrimentally superfluous—because the active mask automatically ensures the prevention of a floating substrate.

As illustrated in Figure 31, small amounts of negative voltage applied to the substrate causes an early breakdown. A larger amount of negative voltage shifts the entire curve in the negative direction. Similar effects were observed with a positive bias on the substrate contact. Even when the substrate was grounded—first, by attaching it to SMU3 set to COMMON mode, CONSTANT function and second, by connecting the substrate to the testing unit's built-in ground—the same type of distortion occurred in SCR performance. Grounding the substrate can even be said to produce a more pronounced distortion.

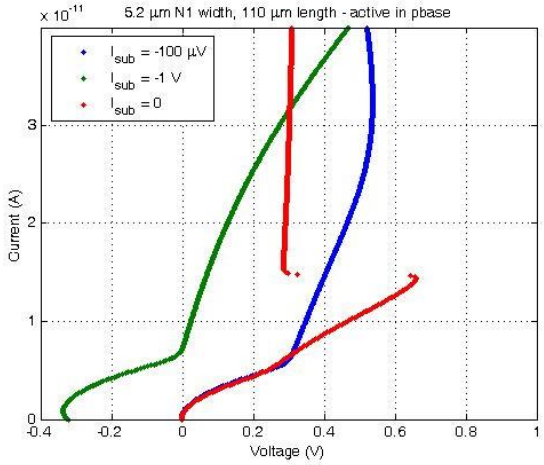


Figure 31. Voltage applied to substrate.

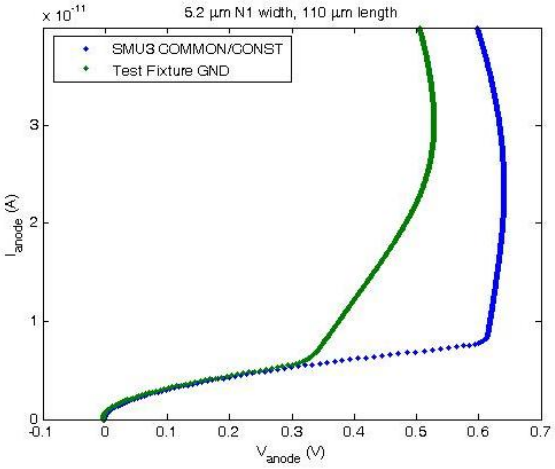


Figure 32. Substrate grounded two different ways.

Interfering with the substrate in any way actually had some lasting negative consequences. The switching voltage for the device measured dropped significantly and wouldn't return to its original value until full chip exposure to light restored the original thyristor I-V characteristics. This restorative effect, however, could not be reproduced in subsequent measurements.

The inconsistency in thyristor performance both before and after substrate manipulations thus prompted a closer look at the interactions between all the devices in the chip and the substrate itself. Of concern was metal layer spacing, which had never been fully resolved before the chip was sent in for fabrication, and the implications of accidental metal layer connections in areas where the two metal types were placed adjacent to each other (refer to Figure 15 in Section B). Contacts had been created for the substrate, so resistance measurements were easily accomplished between the substrate and all layers connected to a bond pad. Table 4 tabulates the results for two chips.

Table 4. Resistance values between chip devices and the substrate.

Primary Chip (MΩ)	Secondary Chip (MΩ)	Affected Layers
5.2	5.2	Collector of transistor w/ no active in pbase
5.1	5.1	Collector of transistor w/ active in pbase
5.2	5.2	Emitter for transistor w/ active in pbase
4.6	4.6	P2 for first five connected SCRs (N1 for last connected SCR)
4.2	4.2	N1 for first five connected SCRs (P2 for last connected SCR)
4.7	4.7	N2 for all connected SCRs
5.0	5.1	N1 for isolated 5.2 μm N1 width
5.2	5.1	N2 for isolated 5.2 μm N1 width
5.1	5.1	N1 for isolated 4.2 μm N1 width
5.1	5.1	N1 for isolated 3.2 μm N1 width
5.2	5.2	N2 for isolated 3.2 μm N1 width

A comparison of the data in Table 4 with the chip layout reveals two things. One, the layers which register any resistance—and hence, a link—with the substrate are all invariably n type layers, regardless of the fact that two metal layer types had been placed directly adjacent to each other even for the p type layers. The doubts raised by the resistance detected in the P2 layer in the first five inter-connected SCRs are nullified by the fact that it connects to the active-enhanced N1 layer of the last inter-connected SCR. The P2 layer for the last inter-connected SCR is conversely connected to the active-enhanced N1 layers of the first five SCRs. Two, only the n layers enhanced with an active mask indicate a link with the substrate, which confirms that the fabricators did not automatically add an active mask coincident with the metal contacts in pbase. Note that N2 in the isolated 4.2 μm N1 width SCR, which didn't behave like a thyristor, registers no substrate association. Note in addition that the emitter of the transistor with no active mask specified in its pbase, which also didn't function properly, likewise displays no substrate association.

One may even argue that the five non-active-enhanced thyristors which share bond pads for their cathode, gate, and N1 contacts only function properly because the last SCR—which has active concurrent with all its metal contacts and was originally

connected to the shared bond pads in a unique manner to facilitate a clean chip design—provides the implementation necessary to compensate for deficiencies in the others.

Concerns about metal layer spacing may still be justified given that there were N1/P2 junction problems in the 5.2 μm and 3.2 μm isolated devices in the secondary chip (not featured in Part 1b). But since the secondary chip registered the same resistances for the same layers as the first chip, and the devices in question still produced thyristor I-V curves, the issue cannot involve an unfavorable connection between the devices in question and the substrate. These SCRs do, however, still connect to the substrate via N1 and N2, and substrate instability caused by measuring the 510 μm length SCR with its P2 wired to the N1 of five other SCRs—and hence to the substrate—would probably affect their performance. This would explain the inconsistent switching behavior noted in the devices in both chips used in the following segments, but the junction issues in the isolated devices in the second chip remain something of a mystery.

d. Gate Current

Measurements for this section were carried out prior to intentional substrate manipulation and were not necessarily executed consecutively. The main goal was to verify that an injection of positive current at P2 serves to augment charge carrier migration across the second junction, causing the thyristor to switch at a lower voltage.

One thing must first be noted regarding equipment usage. Entering a negative constant current on the Agilent 4155B 'Measure' page is the same as instructing the machine that it should create a negative terminal at the specified SMU. In other words, if the goal is to inject positive current into the P2 layer, then the corresponding SMU has to be set to a negative value.

An active-enhanced isolated 5.2 μm N1 width SCR was subjected to both positive and negative current at the P2 layer with the above-mentioned goal in mind. As illustrated in Figure 33, the device does switch at a lower voltage with an injection of positive current and at a higher voltage with an injection of negative current.

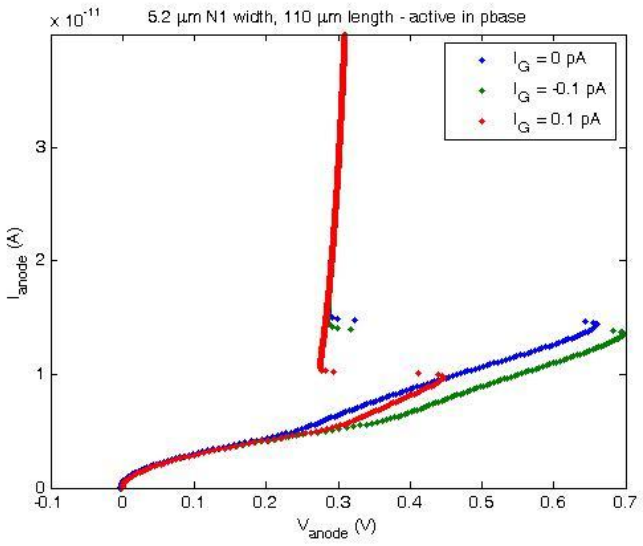


Figure 33. SCR switching under varying gate current.

e. Exposure to Light

Exposing the P2 layer to light is theoretically the same as applying current to the gate. In the former case, electron-hole pairs are generated which then augment the charge carrier migration across the reverse-biased middle junction. The second case, validated in the previous section, relies on the fact that positive current injected directly into the P2 layer augments charge carrier migration across the middle p-n junction.

As an optical detector, then, a thyristor can be stimulated either through the injection of current at the gate contact via a photodiode or through the direct exposure of the chip to light. The first approach could not be illustrated due to the unavailability of a photodiode that could generate photocurrents below the operating range of the fabricated SCRs. The SCRs have I-V characteristics in the pA range, but the lowest obtainable photocurrent is in the nA range (see Figure 36).

To verify the second approach, the Test Fixture lid was left open, and for one set of measurements the chip cover was peeled off and the device itself exposed to ambient light. A second set of measurements was done on the same thyristor in a different chip since the experiments conducted in Part 1c—performed after the first set of measurements in this section—rendered the thyristor unstable.

In Figure 34, one can see that direct light exposure apparently overwhelmed the SCR being tested. The thyristor was subjected to various ambient light intensities achieved through a small range of Test Fixture lid heights. Note that the cover on the chip was removed to expose the device. Normal SCR behavior did not occur even with exposure to the weakest light power (3 nW). The vertical lines which instead resulted could be indicative of very high sensitivity to light that is not altogether unreasonable given the fact that the device's operating range is on the order of 30 pA.

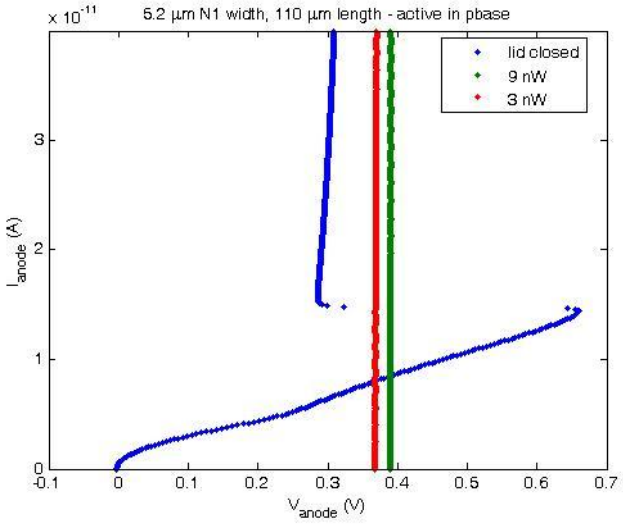


Figure 34. SCR exposed to ambient light. Chip cover off.

Figure 35 is of the same thyristor on a different die whose cover was left on to preclude overwhelming the SCR with light. Device performance with this setup did become more consistent with theory. As expected, the highest lid height with its correspondingly higher incident light power translated to a lower switching voltage, and the lowest lid height with its correspondingly lower incident light power generated a higher switching voltage. The switching voltage for the unexposed thyristor is, of course, higher than that of either case.

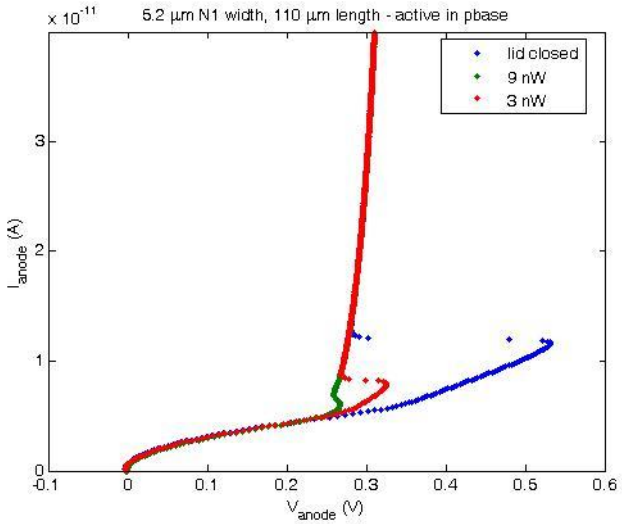


Figure 35. SCR exposed to ambient light. Chip cover on.

In this particular set of characterizations, an alternative measuring approach was taken to remedy the deterioration in thyristor performance which repeated consecutive measurements had made apparent. Assuming that the charges accumulating within the two middle layers were somehow not being discharged fast enough or completely enough between each measurement (2), the grounding outlet on the Test Fixture was substituted for SMU2 at the cathode contact. Consecutive measurements in this configuration had the same effects, which coincides with assertions made by an Agilent representative that setting an SMU to COMMON mode, CONSTANT function is the same as using it as ground (10). However, alternating between SMU2 and the grounding outlet did serve to prevent a gradual degeneration of the switching voltage unrelated to the effects of gate current or light exposure.

Ambient light power was calculated using the equation for responsivity,

$$R = \frac{I_p}{\Phi_p}$$

in which I_p represents the photocurrent and Φ_p represents the incident power. A PDB-V113-ND cerium photodiode was measured by itself to determine the photocurrent levels associated with each lid height (see Figure 36). The responsivity was obtained from

device specifications posted by the manufacturer Advanced Photonix. Typical responsivity was listed as 0.7 A/W for wavelengths between 350-1100 nm with the peak at 950 nm.

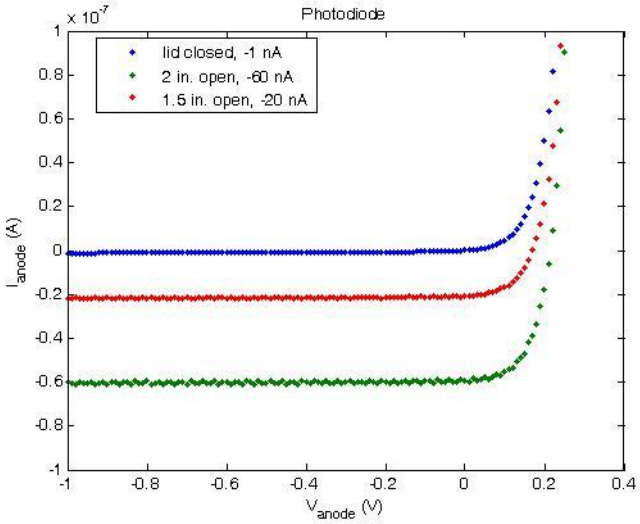


Figure 36. Blue cerium photodiode. Varying degrees of exposure.

f. Sensor Circuit

The final feasibility test is device performance in a circuit designed for optical detection. Although there were no real expectations of any of the SCRs functioning properly in such a circuit—substrate manipulations (both intentional and unintentional) having introduced instability and unresolved junction problems in the isolated devices in the secondary chip having reduced device performance—this segment was added on the chance that expectations might be exceeded and that some insight could be gained from the endeavor.

The isolated 5.2 μm N1 width SCR with a 110 μm length was chosen for the pulse height that it can generate, which Figure 25 indicates is larger than that generated by the 3.2 μm width SCR. This approximation can be derived from an analysis of the circuit described in Figure 1 of Chapter I where

$$V_{DC} = V_{SCR} + V_R \, .$$

V_{DC} is the applied bias, V_{SCR} is the voltage across the SCR, and V_R is the voltage drop across the resistor. Figure 25 indicates that the switching voltage is about 0.7 V, which

means that with a 7.5 V bias, the baseline—a.k.a. the voltage drop across the resistor—should be approximately 6.8 V. The pulses generated with the SCR kept at its switching point should, therefore, have a pulse height of about 0.7 V.

Since the circuit elements are in series,

$$V_{DC} = V_{SCR} + I_{SCR}R$$

where I_{SCR} is the current across the thyristor. The resistance is then

$$R = \frac{V_{DC} - V_{SCR}}{I_{SCR}}.$$

The resistor value for this circuit was determined by adjusting the load line so that it coincided with the thyristor's switching current and overlapped the negative resistance line on the thyristor's I-V curve. R was calculated to be about 0.5 TOhm (the actual resistor used was 0.47 TOhm). A very small capacitor was naturally needed for a manageable RC time constant, but the capacitance in the cables used to connect to the power source and to the oscilloscope (~5 pF measured) plus the internal capacitance of the oscilloscope itself (~8 pF printed on equipment) rendered the use of a capacitor unnecessary. The RC time constant was determined to be approximately 6.1 s.

For the 5.2 μm N1 width isolated device in the primary chip, the baseline did rise as the bias was increased, but no pulses were generated—or could be detected—at or near 7.5 V, which is where pulsing should have started for the circuit constructed. The same device in the secondary chip produced the same results at its respective values. Pulses for that device were expected at around 5.5 V based on its I-V characteristics, and a pulse height of about 0.4 V was anticipated.

Overall, both outcomes are unsurprising, and both highlight the necessity of improving thyristor design so that there exists some stability in thyristor performance. Additionally, careful attention needs to be paid in the spacing between metal layers.

2. Analysis

In determining the design parameters which would optimize an SCR for optical detection, three factors have been explored. The first factor is the presence of an active mask at all metal contacts—even within the pbase layer, contrary to MOSIS

documentation—and whether or not its absence does indeed cause noticeable deficiencies in thyristor behavior. The second factor is the N1 width, and the third factor is the thyristor length. Device behavior was then tested for proper response with direct application of current at the gate contact and with device exposure to light. Finally, the device was incorporated in a sensor circuit to address the issue of its practicality as the main component of an optical sensor. The ultimate result of all these tests and measurements is a confirmation that the ideal SCR used in optical detection incorporates an active mask under all metal contacts and has an N1 width of at least 5.2 μm—preferably more—but the ideal device length is a parameter that needs further investigation.

The detrimental effects associated with the absence of an active mask in conjunction with metal contacts were manifested without a doubt in two devices. In the transistors, its absence was marked by erratic and erroneous behavior in one device compared to a more uniform and recognizable characterization in the other device. In the SCRs, its absence was most conspicuous in one thyristor's inability to undergo reverse resistance before turning on. Though six SCRs were actually fabricated without the active mask within pbase, and only one failed to perform properly, the five that could perform as a thyristor were inter-connected with one active-enhanced thyristor in such a way as to overcome the deficiencies associated with their flawed layout composition.

This notion is further validated by an inspection of the p-n junctions in the defective transistor. The appropriate I-V curve for a p-n junction could not be generated between the base and the collector and between the base and the emitter. The base and the emitter for that particular transistor were both laid out without an active mask at the metal contacts.

Moreover, the results of an investigation into the link between the chip substrate and all the devices within the chip confirms that the active mask is key in preventing the substrate from floating and hence, in ensuring device functionality. In the isolated devices that performed properly, resistance was detected between the substrate contact and all n type layers with active, indicating a link between those layers and the chip's substrate. On the other hand, in the isolated devices that did not work, no resistance

registered between the substrate and the n type layers lacking active—i.e., the emitter in the transistor and N2 in the defective thyristor. The fact that this absence coincides with the inability of the two devices to perform properly further substantiates the claim that all metal contacts should be implemented by an active mask (6 p. 128).

Regarding N1 width, device functionality can be ensured by a conservative treatment of the design rules. The fabrication process is uncertain enough in execution that a width specified during layout may not be the actual width produced, so a proposed N1 width of 3.2 μm—which is the minimum recommended spacing in the SCMOS process between pbase and active (5 p. 59)—may actually result in an N1 width less than 3.2 μm (2). In cases where design rules are broken, the chances of a device operating properly are reduced (6 p. 125), and this predicted unreliability immediately makes this particular width an inappropriate choice for sensor design. N1 widths at least 2 μm wider would boost the reliability of device performance without grossly hindering design flexbility. Thyristor design should therefore focus on an N1 width equal to or exceeding 5.2 μm.

The matter of optimal device length, however, is not as conclusive. Decisions made during chip layout resulted in the fabrication of no isolated thyristors with lengths longer than 110 μm, and the one long thyristor that was fabricated with the proper layout had been connected to faulty devices in such a way as to compromise its performance. While this oversight proved fortuitous in uncovering the relationship between the active mask and the chip substrate, it removed any opportunity for verifying that a longer thyristor length translates to a higher current operating range. Higher current ranges would eliminate the need for a tera-Ohm resistor in the sensor circuit. Moreover, higher current ranges would lessen device sensitivity, which may be desirable in some sensor designs. Thyristor lengths longer than 110 μm should therefore be explored.

By and large, this project imparts an assurance of the possibility of an optical detector conceived around a customized thyristor. Measurements in Part 1d confirm that the fabricated SCR will indeed switch at a lower voltage with gate current, and measurements in Part 1e show that the SCR is sensitive enough that direct exposure to

light will have the same effect as applying gate current. In practice then, the pulses that the device should generate ought to have inter-pulse durations that decrease as light intensity is increased (1).

In reality, however, putting this device in a sensor circuit only brought to the forefront the inconsistencies in device performance noticed during consecutive measurements and especially after intentional substrate biasing. If the thyristor's I-V characteristics fluctuate, then its feasibility as a detector is compromised because the bias will never be set. That these inconsistencies were brought about due to substrate biasing is probable but not completely so. In any case, the optimal device parameters and layout configurations discussed above will likely resolve these inconsistencies, and then there is every expectation that the viability promised by favorable device response under two types of illumination will be manifested in a sensor circuit that does what it has been designed to do.

III. CONCLUSIONS

This thesis has attempted to resume past endeavors at the Naval Postgraduate School to develop an optical detector driven by a silicon controlled rectifier. What started as a discovery by Professor Gamani Karunasiri of the potential of a thyristor to register the presence of light through pulse generation (1) has developed into an investigation into the dimensional parameters of a thyristor which would optimize its performance as a sensor. In this latest iteration of research on the subject, not only have optimal parameters been identified, a new understanding of the CMOS fabrication process has also been obtained which will greatly aid in developing fully functional thyristors in subsequent fabrication runs.

LT David Moore's work dealt primarily with modeling thyristor behavior in order to identify the parameters that would have the greatest effect on thyristor performance. The first n doped layer became a focus of interest since variations in its width strongly affect the thyristor switching voltage but do not dramatically change the switching current (5). Specifically, the layer width is directly proportional to the switching voltage. A wider N1 width can then be expected to result in a thyristor that generates more easily detectable pulse heights, but its operating rage will remain generally the same. To test his findings, Moore submitted thyristor designs for fabrication, but his orders to NPS expired before he could analyze the devices he created.

In this thesis, Moore's thyristors were analyzed and found unfeasible mainly due to an accidental metal layer connection. While trying to fix the chip layout, conflicting advice was received regarding the active mask usually excluded from the pbase layer in the SCMOS design process (7). The new layout submitted for fabrication thus incorporated the original SCMOS configuration and a configuration in which active was included with all metal contacts, as typical CMOS design literature suggests (6). An analysis of the thyristors in these new chips confirms the importance of including an active mask with all metal contacts and also validates Moore's conclusions on thyristor behavior derived from his simulations. Namely, the thyristor switching voltage will indeed increase as the N1 width is increased.

Further device testing proved that the introduction of current into the P2 layer through either a photodiode or directly onto the device itself causes a decrease in switching voltage. In the sensor circuit developed by Professor Karunasiri, the bias can therefore be set to such a level that no pulsing occurs unless light is detected by the student-designed thyristors. Though these fabricated thyristors did not actually function in the circuit mentioned, the attempt to create an optical detector did emphasize the importance of implementing all metal contacts with an active mask as a means of ensuring thyristor performance. Furthermore, the process of determining which thyristor was best suited for use in the sensor circuit underscored the fact that 5.2 μm should be the minimum N1 width included in subsequent thyristor design since shorter widths foretell the increased possibility of device unfeasibility.

Those same experiments on thyristor behavior with light exposure also introduce the idea that a higher current operating range may be desired for some sensor designs. However, Table 1 in Chapter I indicates that increasing the N1 and the P2 widths might not be sufficient. Device length is therefore the one parameter that will likely have the biggest effect on operating range. Since the present chip layout prevents the opportunity to examine the exact impact this parameter really has, subsequent work on the subject of thyristor-based optical detectors should accordingly expend some effort toward determining optimal device lengths.

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